A Dynamically Reconfigurable ECC Decoder Architecture for the next generation communication standards (5G, SDR and beyond…)

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Université Bretagne Sud

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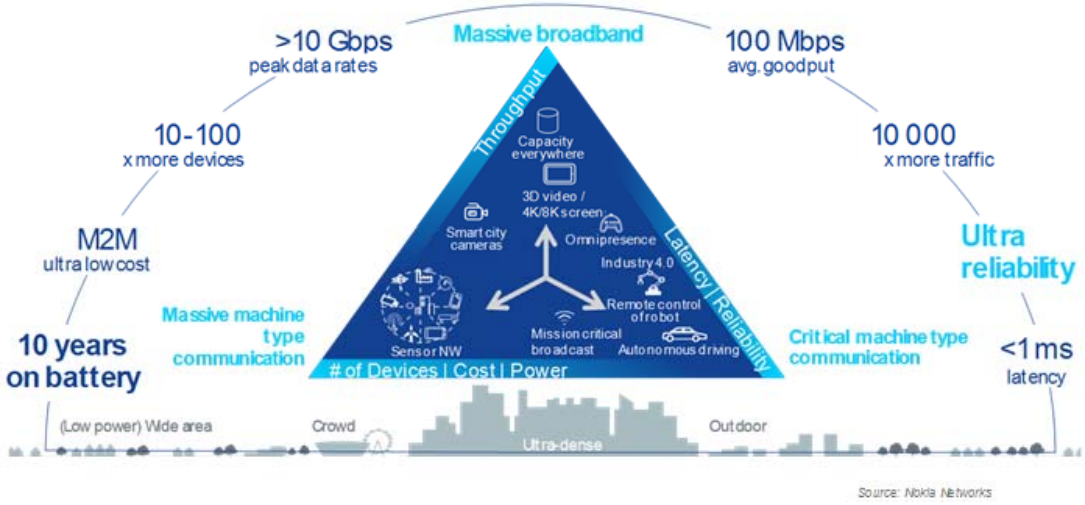
Lab-STICC

Context

A Widely Interconnected World

- **Incoming communication standards will be the origins of a deep revolution for the future**
  - 5G, Software Defined Radio, Cognitive Radio…
  - New communication scenarii
  - Internet of Things
  - …

- **Convergence of communication networks**
  - Several physical layers
  - Several communication protocols (Wi-Fi, LTE, RFID tags...)
  - ...



Interconnected Battlefields

- **Military users benefit from access to real-time data**
  - Improved situational awareness
  - Flexible networks
  - Increased level of autonomy
  - Reduced equipment sizes

Source: Thales

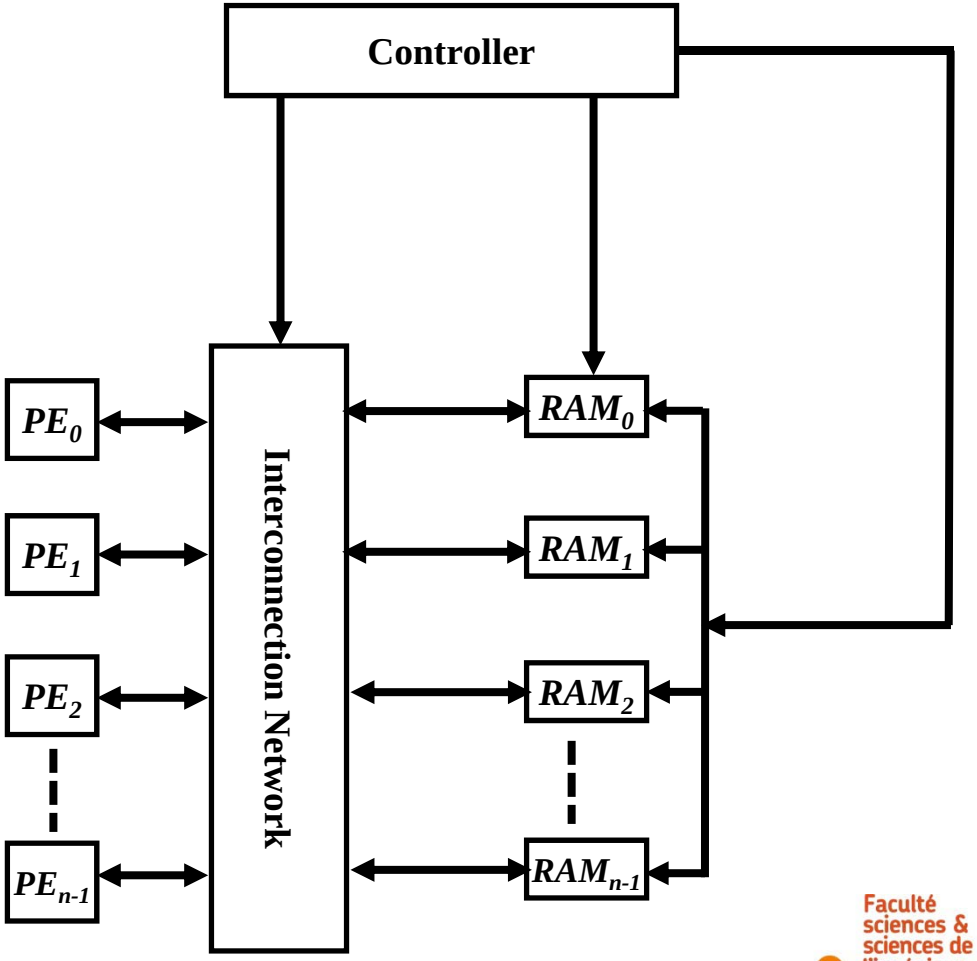
- **Reliable networks and high-throughput communications**

- **Evolution of Networked Communications**

Channel Coding/Decoding is the Key

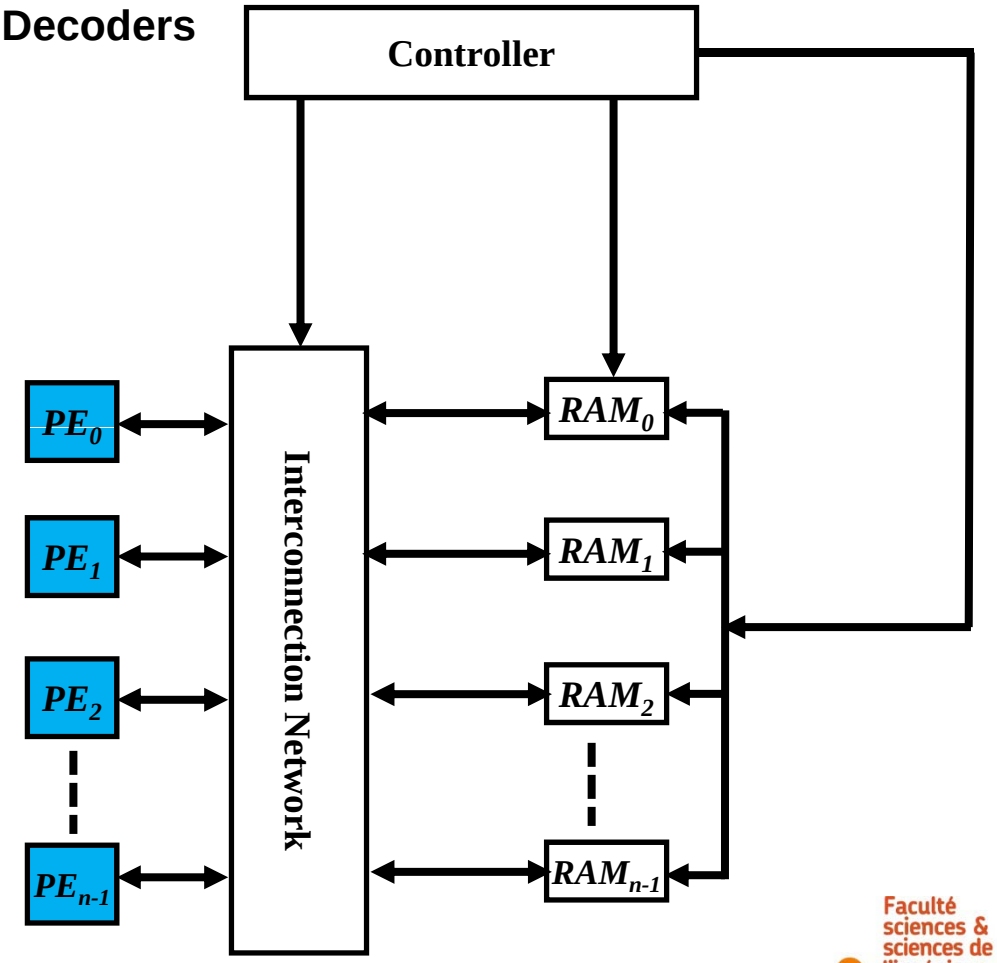
- **FEC (Forward Error Correction) architecture is a critical element**
- **Impacts**
  - Quality of Services
  - Power Consumption
  - Efficiency of radio resources usage
  - Interoperability
  - …
- **FEC decoders comes at the expense of huge computational complexity**
- **In order to limit costs** (development, energy, amount of required equipments…)
  - Adaptive architecture
    - Various Throughputs/Latency targets
    - Several types of FEC codes (Turbo Codes, LDPC, Polar codes...)
  - Dynamic System *(i.e. During execution)*

Typical FEC Architecture



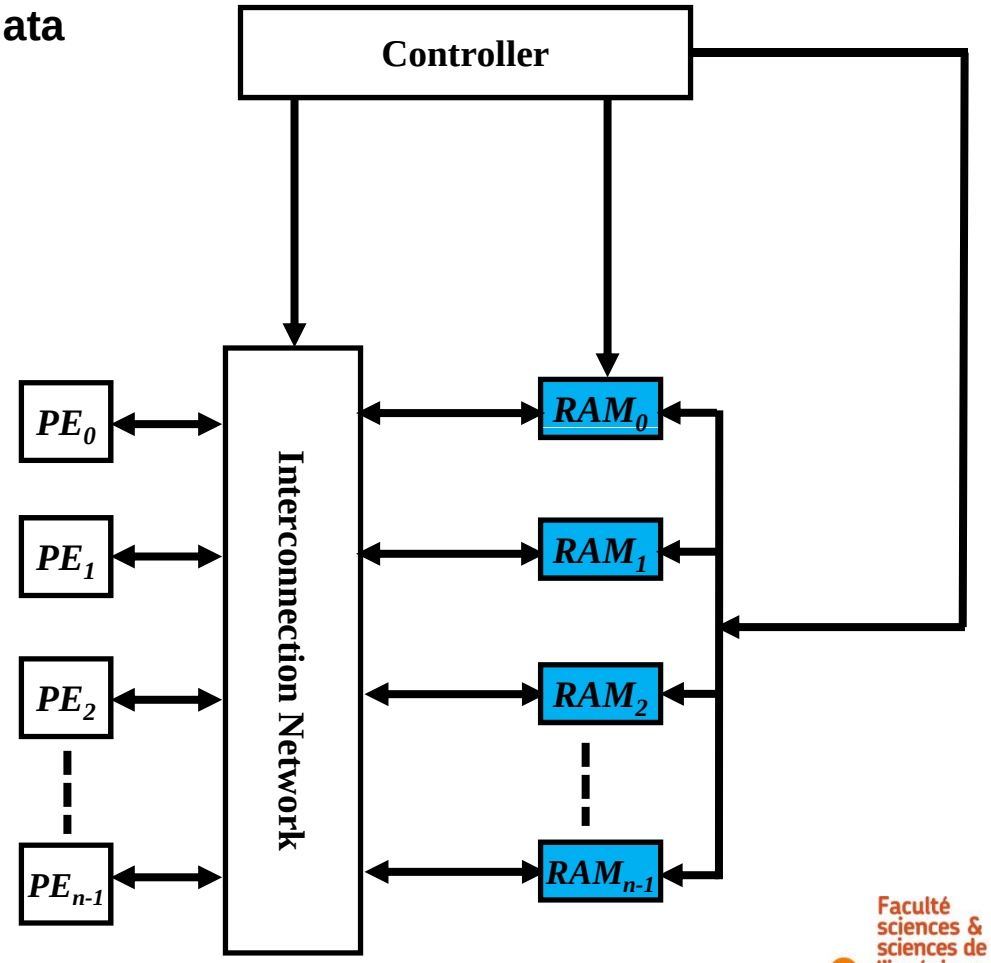
Typical FEC Architecture

- **Processing Elements or Decoders to process data**



Typical FEC Architecture

- **Memory banks to store data**



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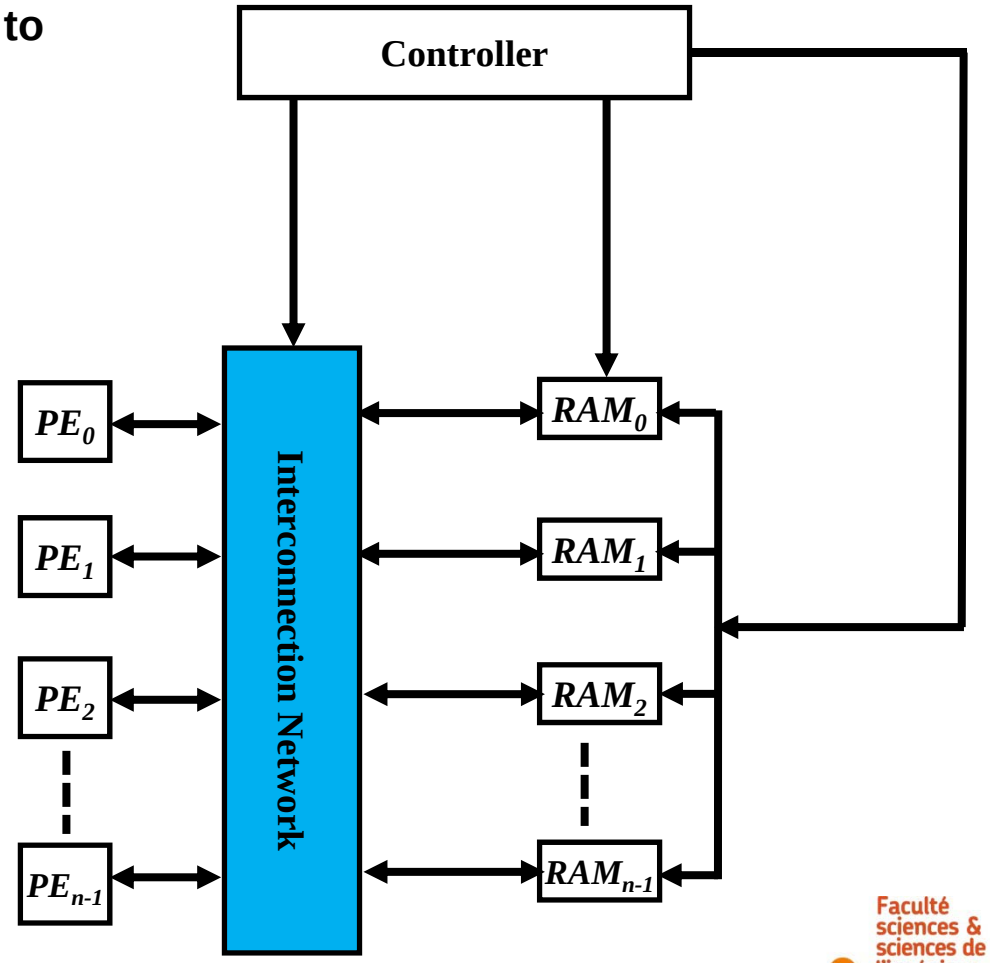
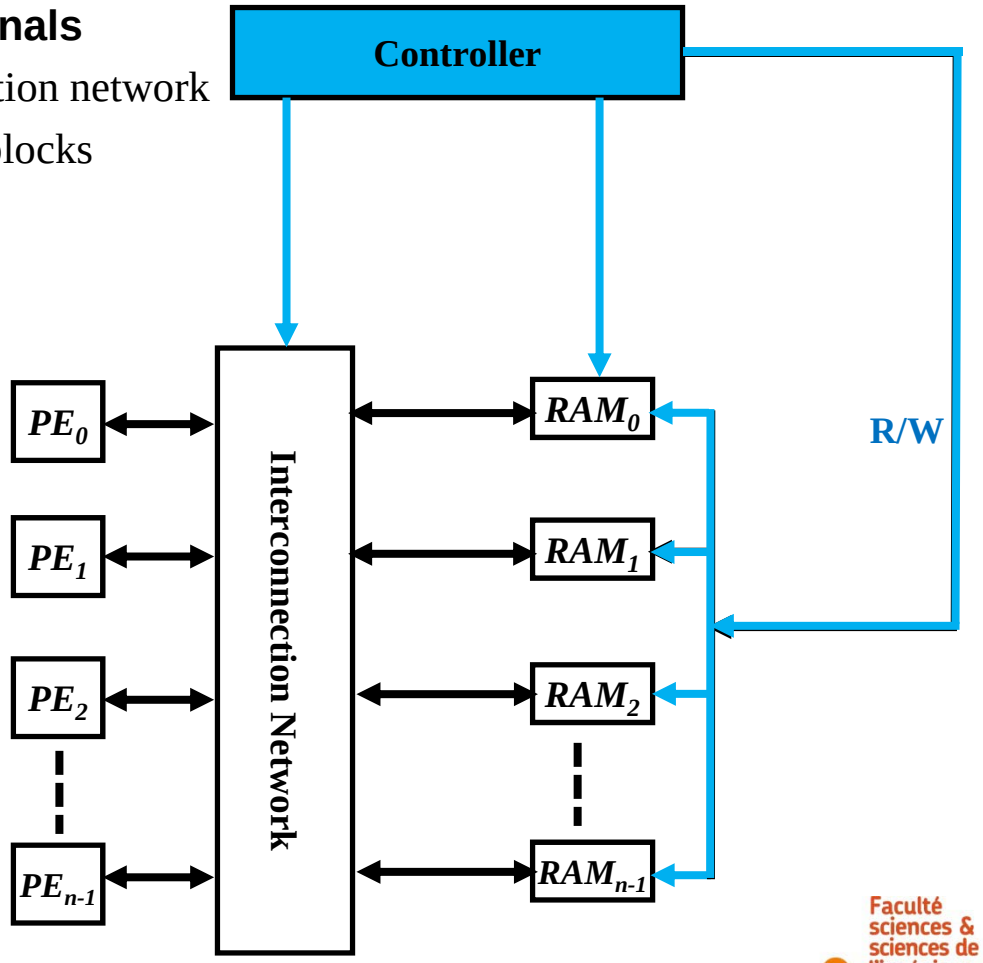
Typical FEC Architecture

- **Interconnection network to connect *PEs* to *RAMs***

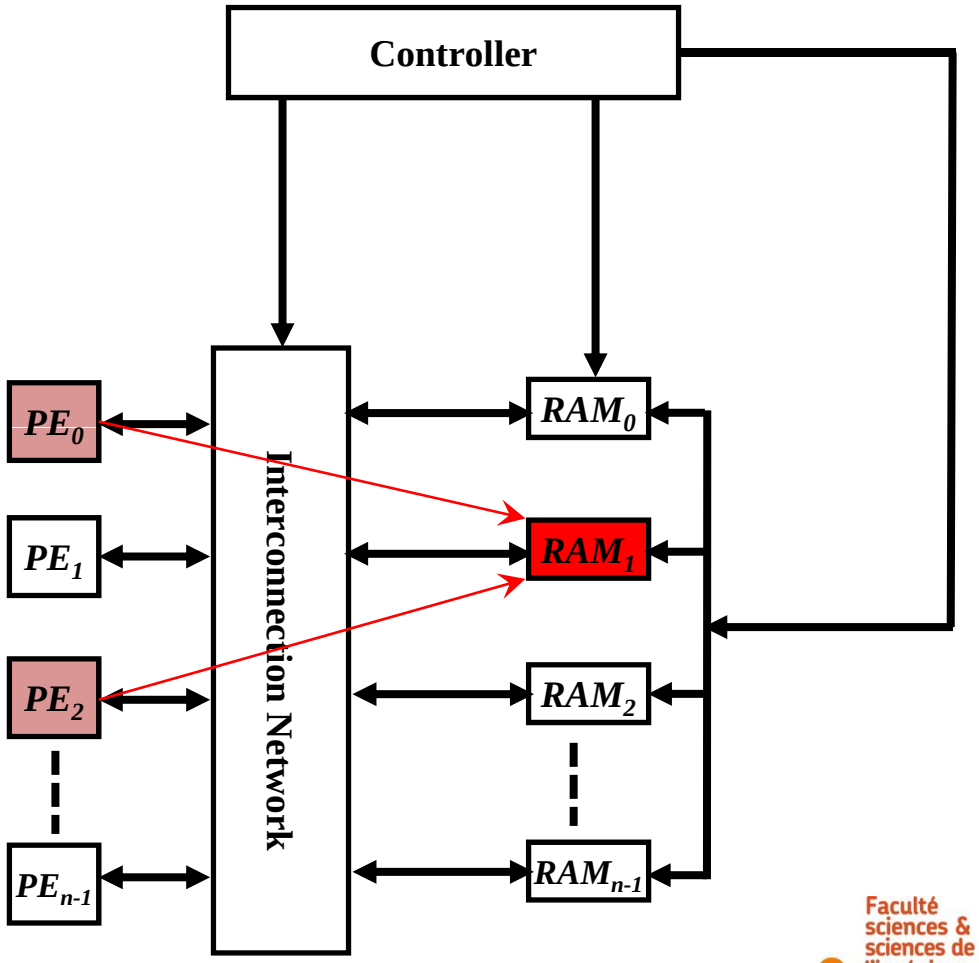


Typical FEC Architecture

- **Generation of control signals**
  - To pilot the interconnection network
  - To handle the memory blocks *(Address, R/W…)*

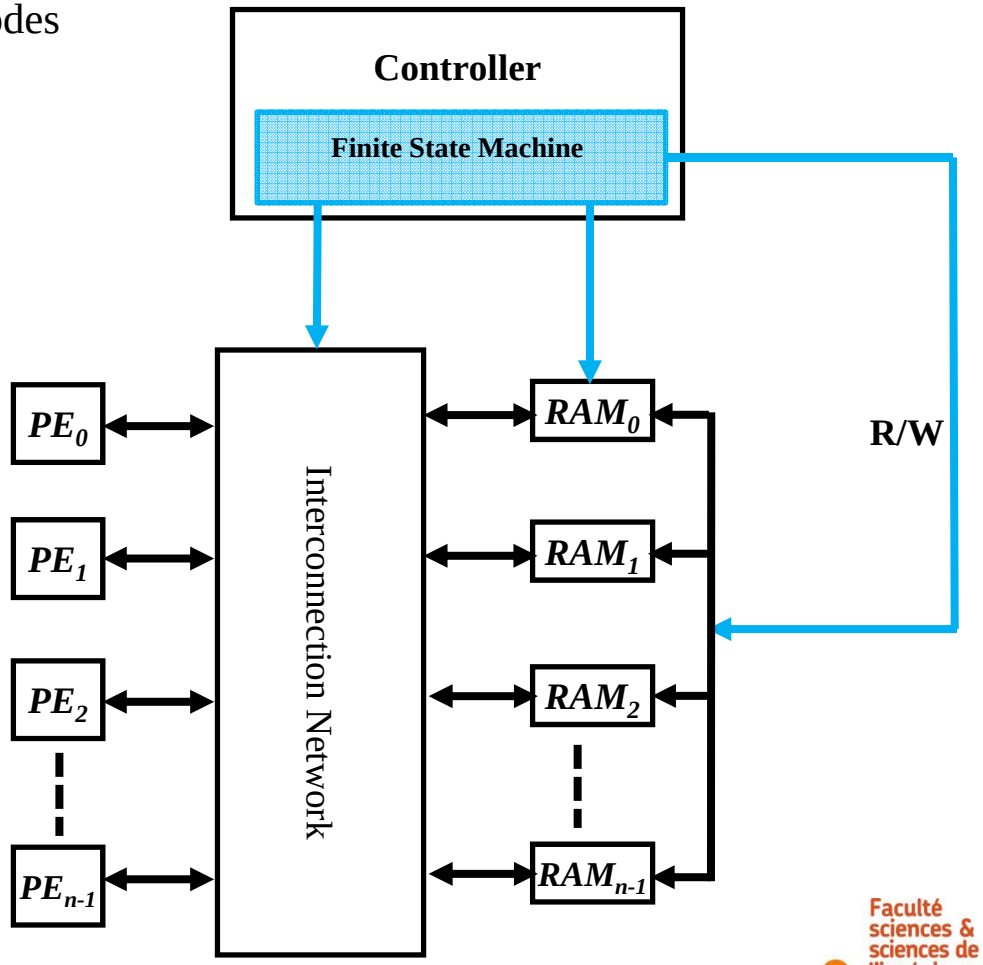


Parallel Memory Access Conflicts



Natively conflict free interleaver

- **Defining a conflict free interleaving law**
  - Multiple slices Turbo codes
  - QPP interleaver (LTE)
  - Structured LDPC codes (WIFI, WiMAX)
- **Pros**
  - Possible use of a simplified interconnection network
- **Cons**
  - Dedicated to specific interleaving law
  - Only for a sub-set of parallelism
  - Channel interleavers still have conflicts
  - Not a multi-mode architecture



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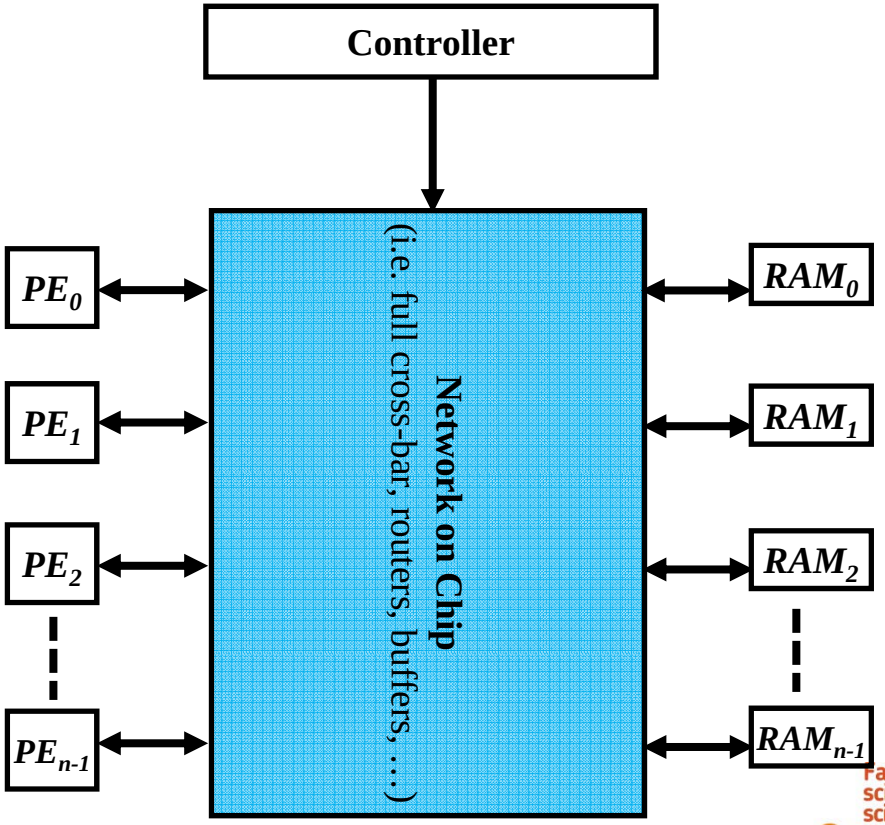
Online Conflict Resolution

- **Storing All Data Access**
  - Including conflicts resolution memory mappings
- **Pros**
  - Generic approach
- **Cons**
  - Buffers sizing through simulations
  - Increased architectural cost
  - Increased latency
  - Not a multi-mode architecture



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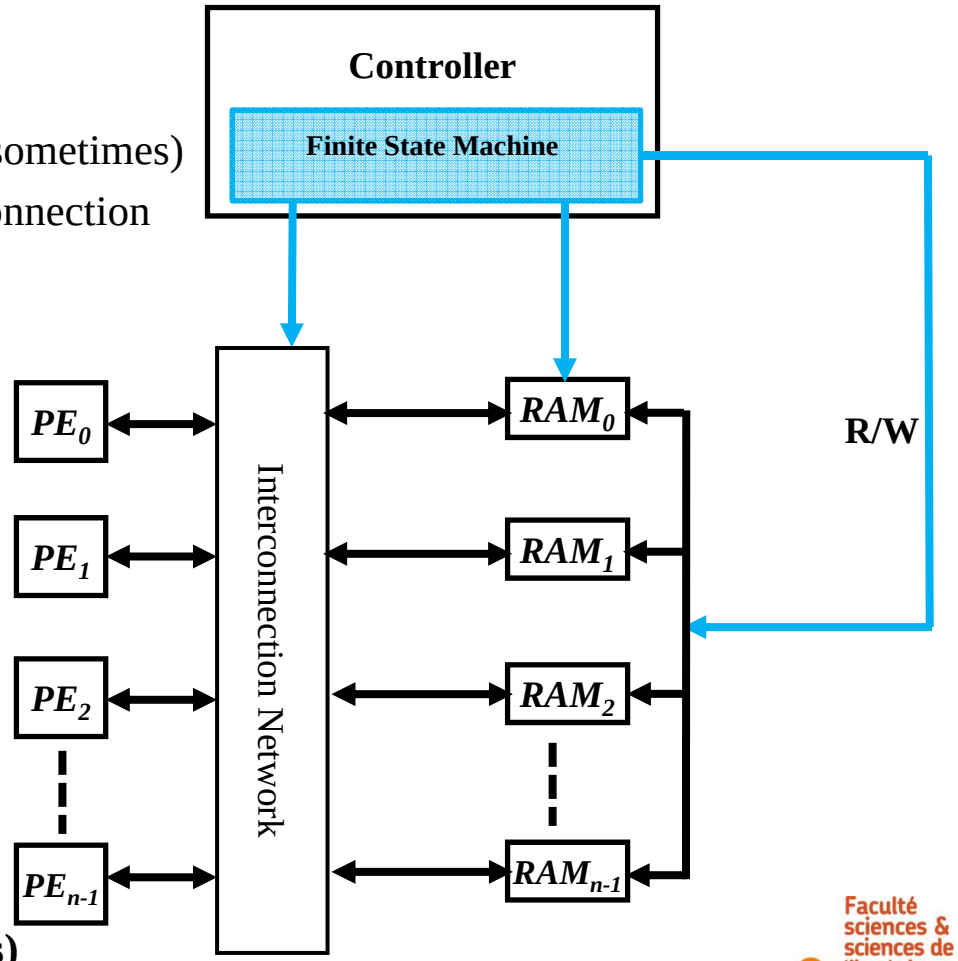
Design Time Conflicts Resolution *by hand*

- **Find a conflict free memory mapping**
- **Pros**
  - Network cost reduction (sometimes)
  - Respect a targeted interconnection network (sometimes)
- **Cons**
  - No controller cost optimization
  - Not a generic approach
  - Not a multi-mode architecture
  - Some approaches need additional memory
  - **Extremely time consuming (i.e. several man/months)**

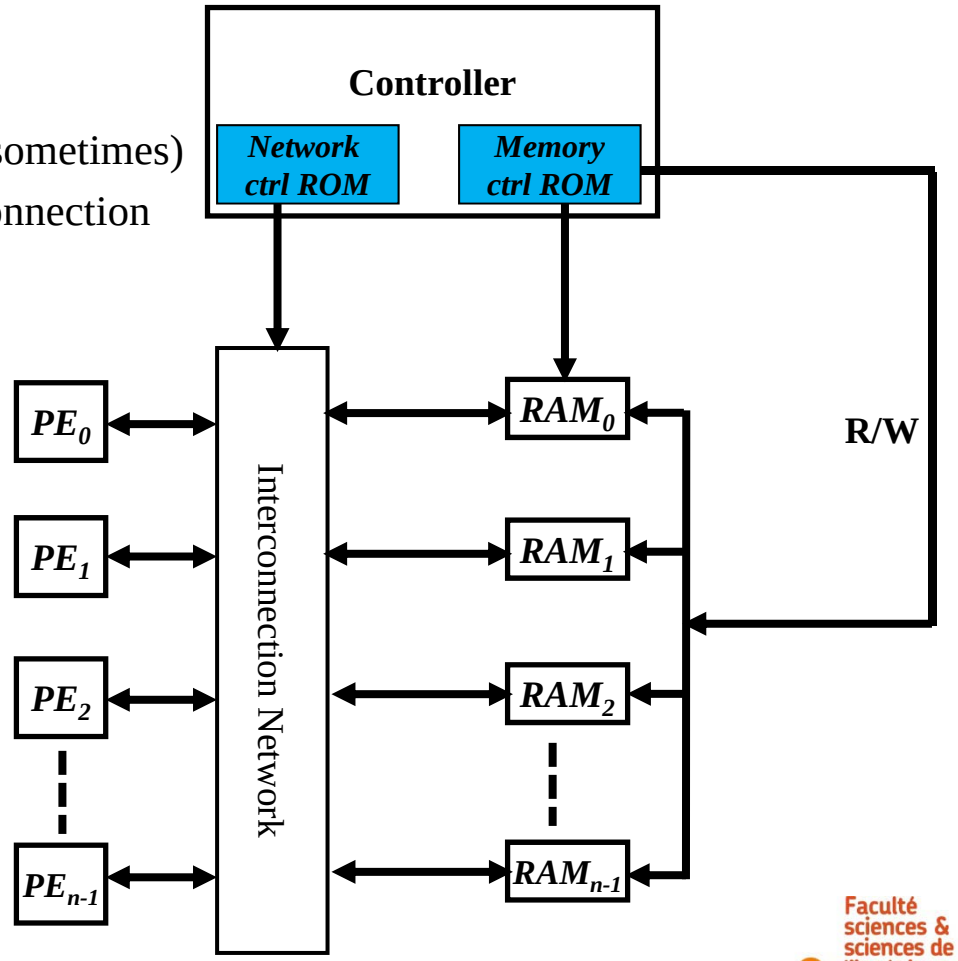


Design Time Conflicts Resolution *automatic*

- **Find a conflict free memory mapping**

- **Pros**
  - Network cost reduction (sometimes)
  - Respect a targeted interconnection network (sometimes)
  - **Reduced design time**

- **Cons**
  - No controller cost optimization
  - Not a generic approach
  - Not a multi-mode architecture
  - Some approaches need additional memory



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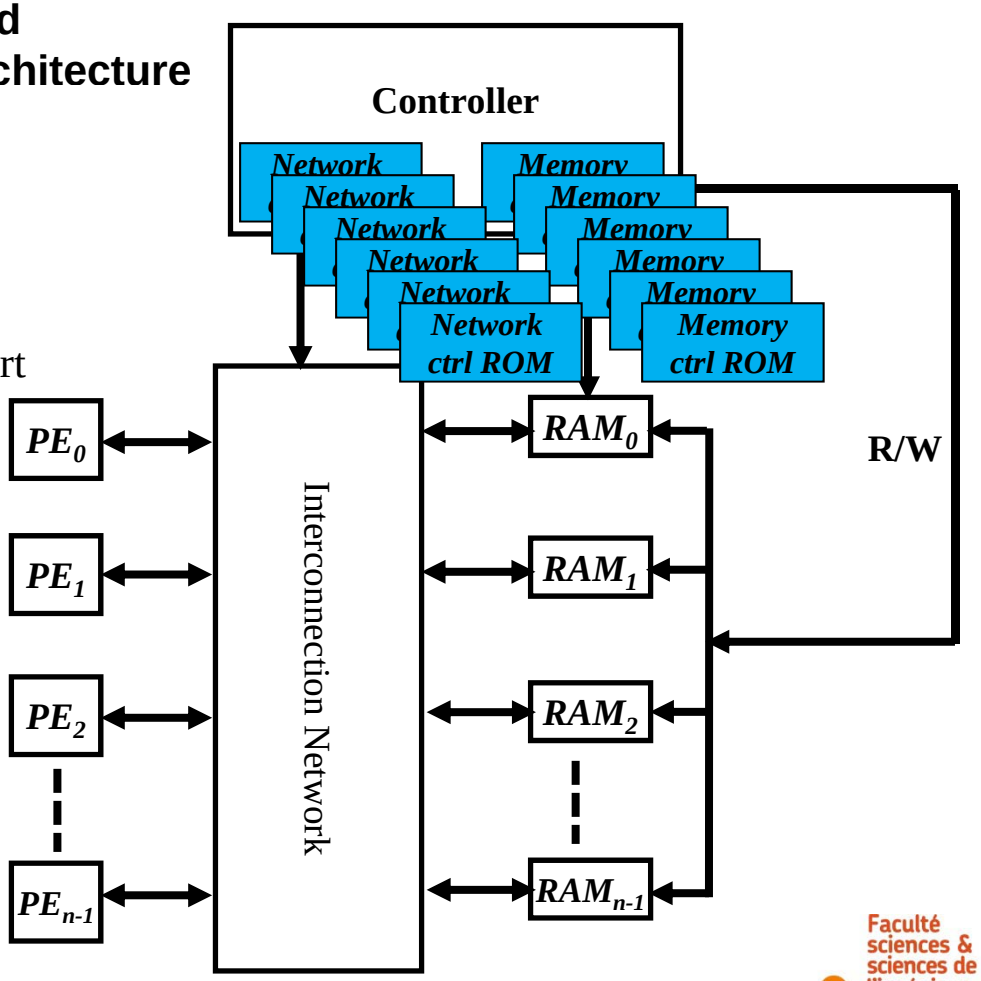
Multiple Block Lengths/Standard Support

- **Multiple ROMs are required, one for each block lengths, and this for each standard supported by decoder architecture**
- **Pros**
  - Adaptive architecture
  - Adaptive behavior
  - Multiple standard support
- **Cons**
  - **Complex network**
  - **Huge memory cost**
  - **Power hungry**



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GRAAL – Adaptative Architecture for Online Memory Mapping

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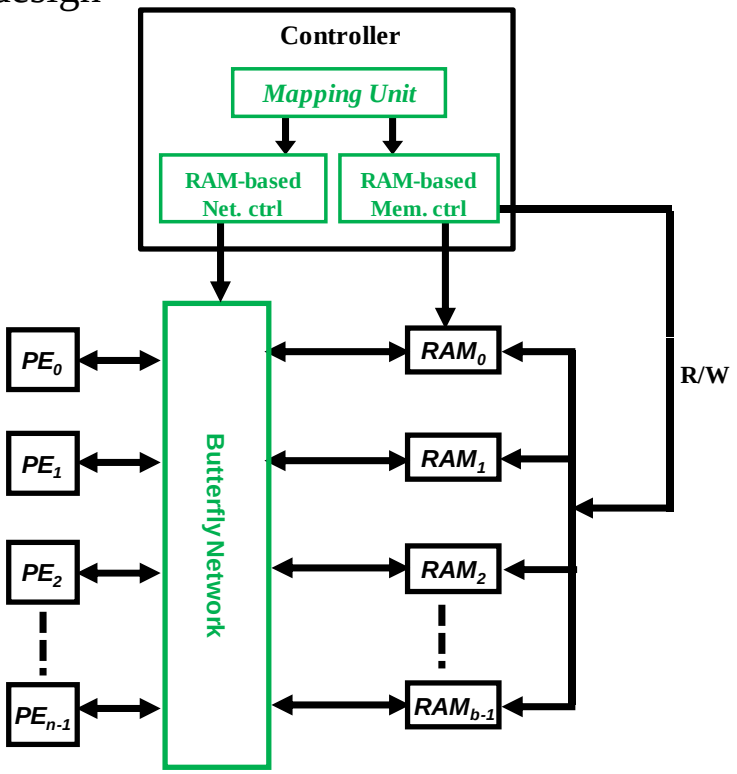
GRAAL Patented Architecture

- **To design an architecture that is able to deal with**
  - Multiple block lengths & Any standards
  - Reduced architectural cost (i.e. simple regular interconnection, reduced control…)
  - Reduced power consumption
  - Switch from one configuration to another on-the-fly (i.e. block length, standard…)
  - Our goal : ASIC design



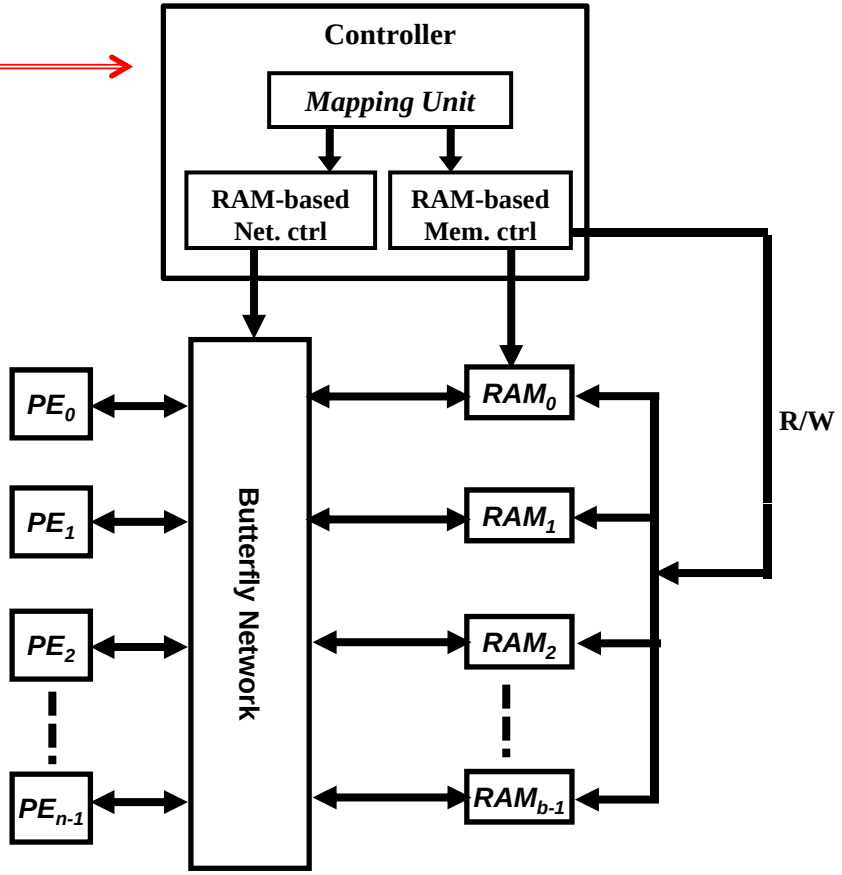
Patent no. FR12.51688

GRAAL Scenario

- **The architecture is decoding a given block from LTE (e.g.)**

First configuration

LTE standard
block **#40** data
& Input data order
PE Parallelism = **2**
RAM Parallelism = **2**

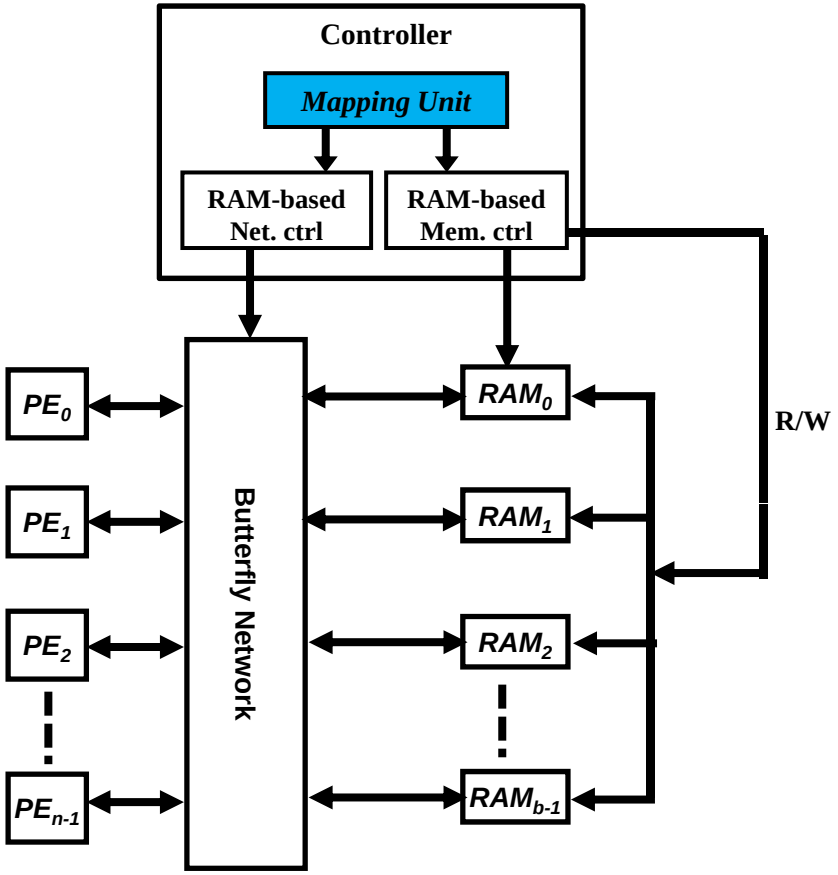


A.H. Sani, S. Ur Reehman, C. Chavet and P. Coussy, "A First Step Toward On-Chip Memory Mapping for Parallel Turbo and LDPC Decoders: A Polynomial Time Mapping Algorithm", **IEEE Transactions on Signal Processing**, Vol 61 - 2013, Issue: 16

GRAAL Scenario

- **First the Mapping Unit generates a *Virtual Mapping***

LTE standard
block #40 data
& Input data order
PE Parallelism = 2
RAM Parallelism = 2



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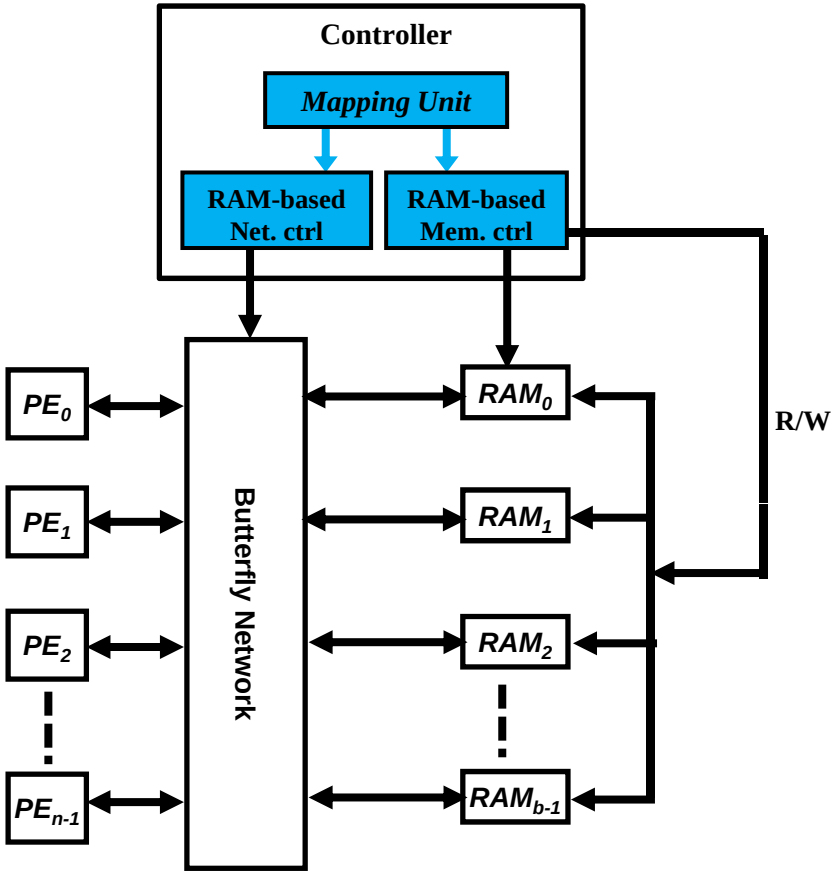
GRAAL Scenario

- **Then, the Mapping Unit generates the final control signals for the network and the memories from this *Virtual Mapping***

LTE standard
block #40 data
& Input data order
PE Parallelism = 2
RAM Parallelism = 2

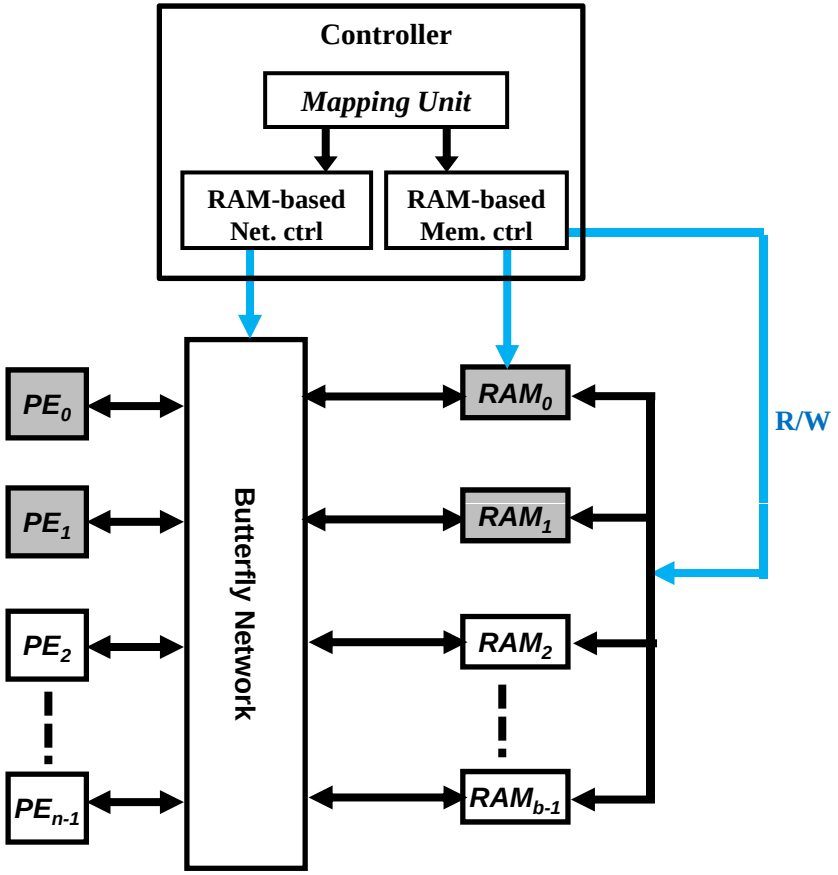


Book: C. Chavet and P. Coussy Editors
"Advanced Hardware Design for Error Correcting Codes", **Springer-Verlag**, ISBN: 978-3-319-10568-0 (Print) / 978-3-319-10569-7 (Online), 2015.

GRAAL Scenario

- **The processing elements process the data**

LTE communication



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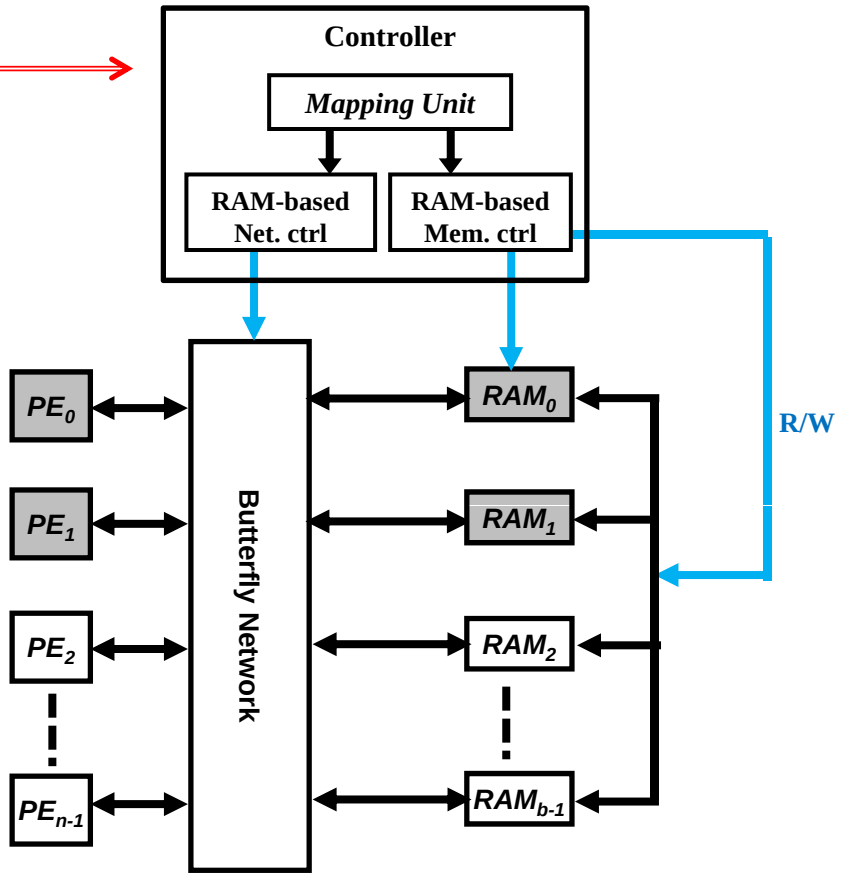
GRAAL Scenario

- **The architecture need to process another block from LTE**

New configuration request

LTE standard
block **#4096** data
& Input data order
PE Parallelism = **n**
RAM Parallelism = **n**

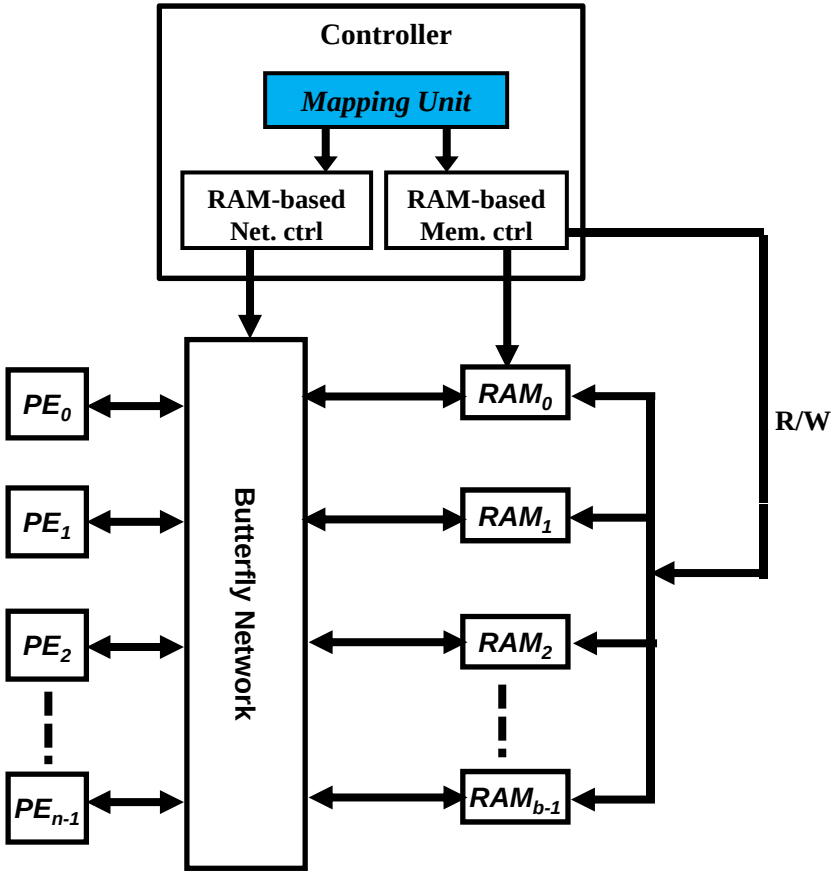


Patent no. FR12.51688

GRAAL Scenario

- **First the Mapping Unit generates a new *Virtual Mapping***

LTE standard
block #4096 data
& Input data order
PE Parallelism = n
RAM Parallelism = n

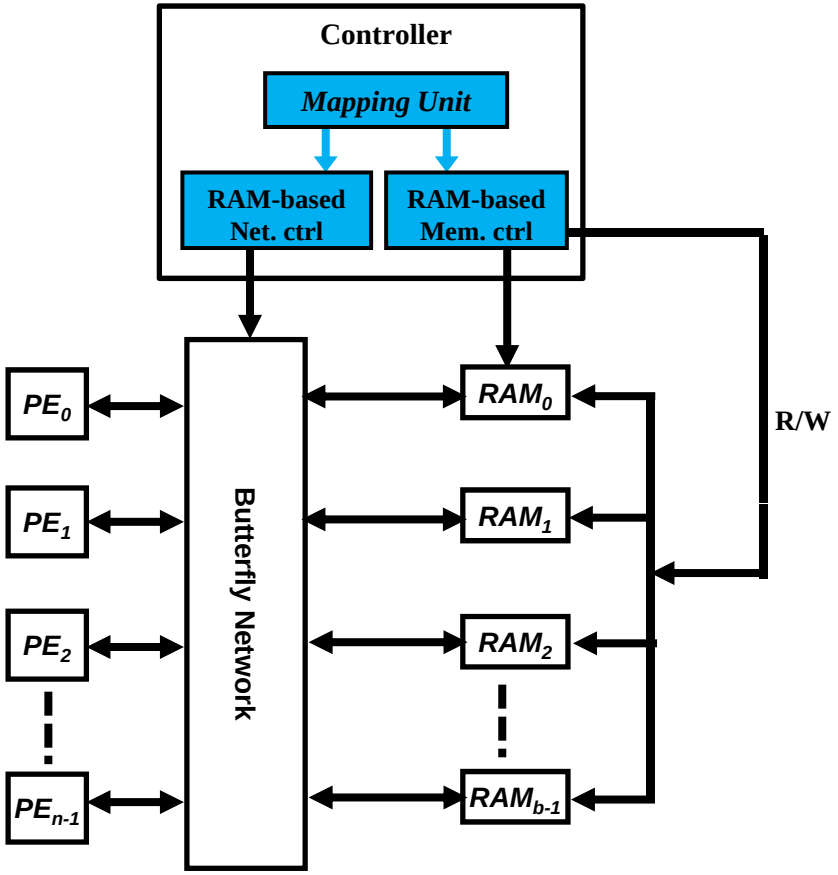


Patent no. FR12.51688

GRAAL Scenario

- **Then, the Mapping Unit generates the new set of control signals for the network and the memories from this new *Virtual Mapping***

LTE standard
block #4096 data
& Input data order
PE Parallelism = n
RAM Parallelism = n



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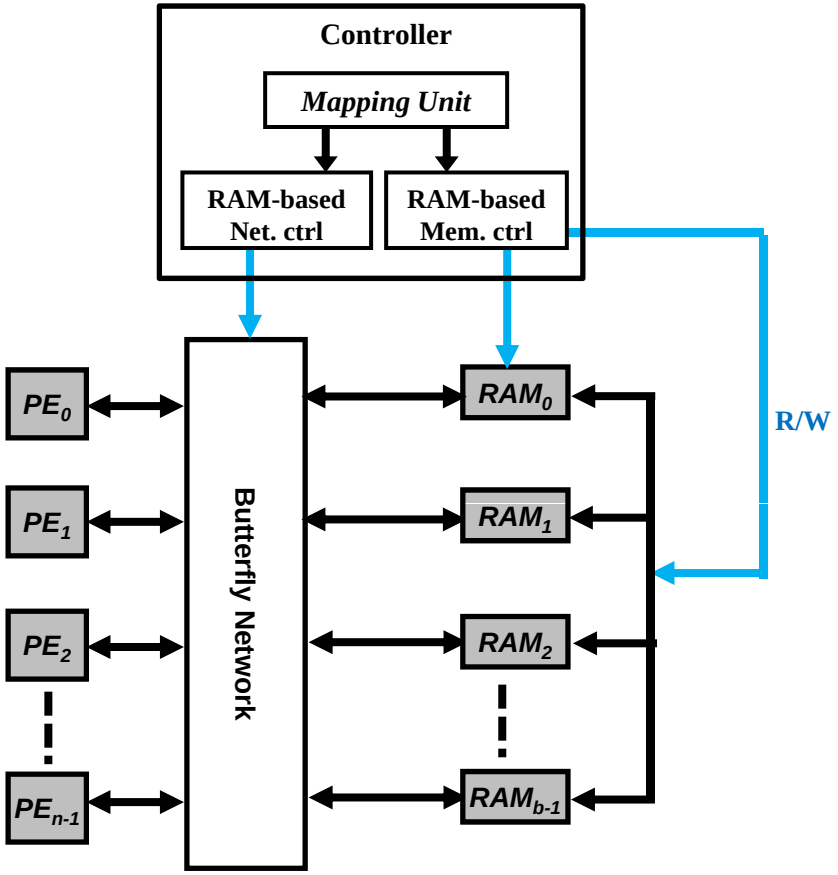
GRAAL Scenario

- **The processing elements process the data**

LTE communication



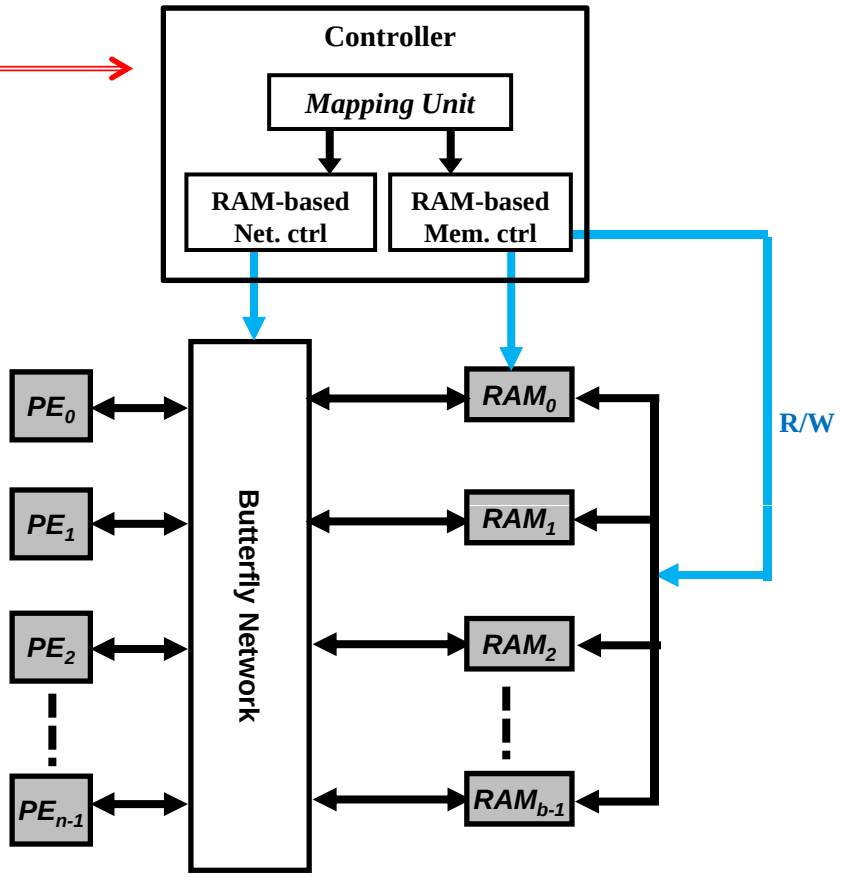
Patent no. FR12.51688

GRAAL Scenario

- **The architecture changes the target communication (e.g. to Wifi)**

New configuration request

WIFI standard
block **#256** data
& Input data order
PE Parallelism = **4**
RAM Parallelism = **4**

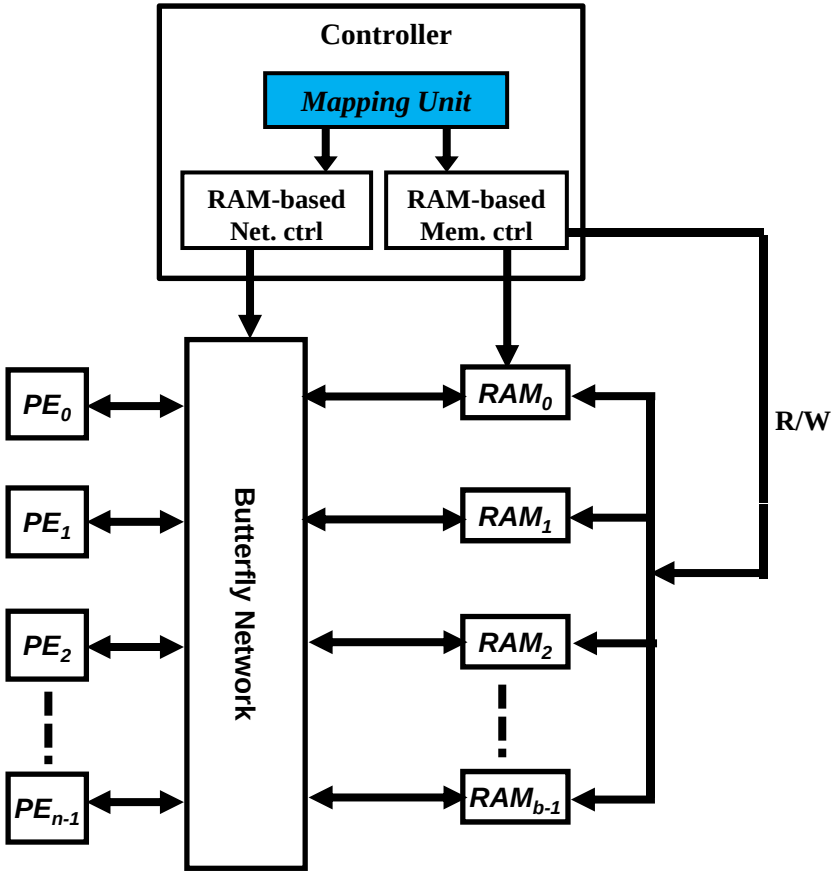


Patent no. FR12.51688

GRAAL Scenario

- **First the Mapping Unit generates a new *Virtual Mapping* from the new constraints**

WIFI standard
block #256 data
& Input data order
PE Parallelism = 4
RAM Parallelism = 4

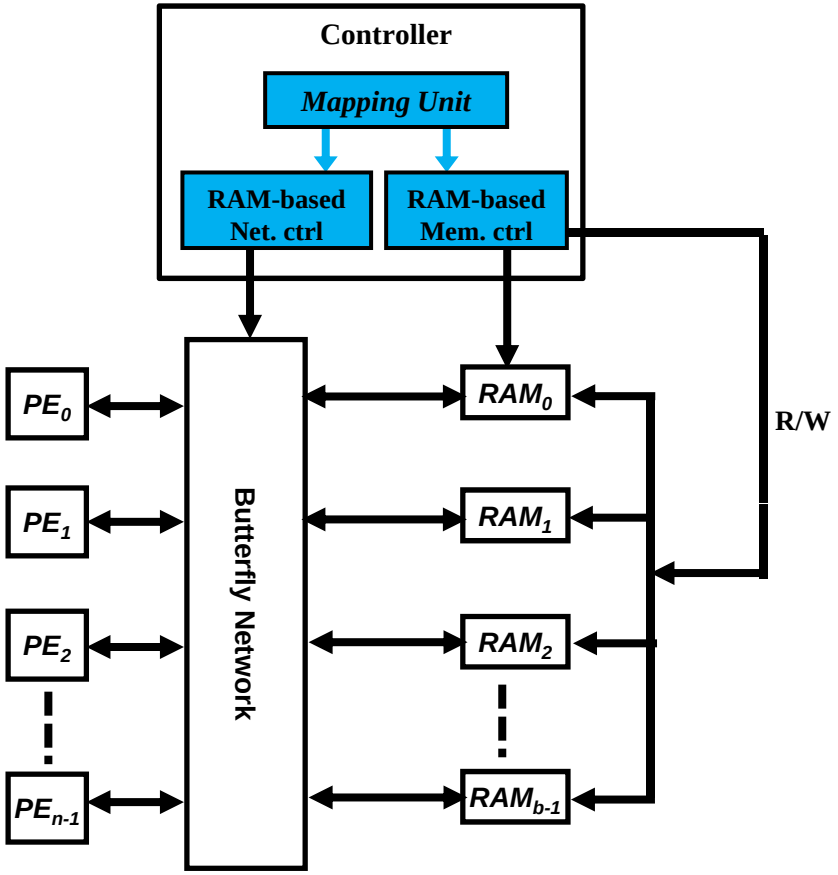


Patent no. FR12.51688

GRAAL Scenario

- **Then, the Mapping Unit generates the new set of control signals for the network and the memories from this new *Virtual Mapping***

WIFI standard
block #256 data
& Input data order
PE Parallelism = 4
RAM Parallelism = 4



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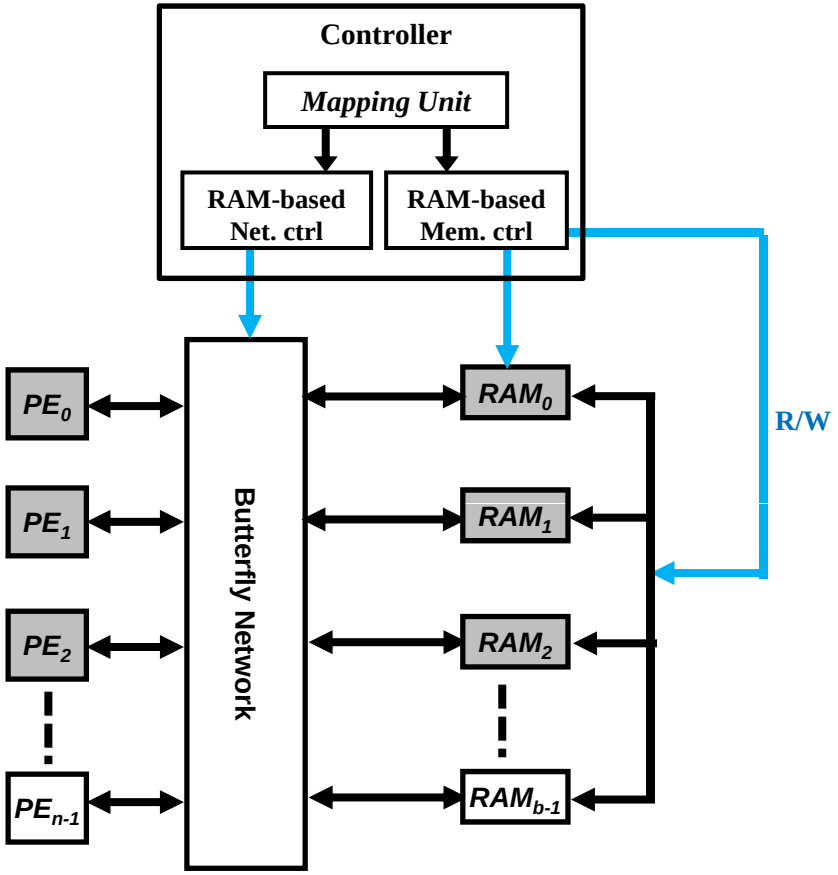
GRAAL Scenario

- **The processing elements process the data**

WIFI communication



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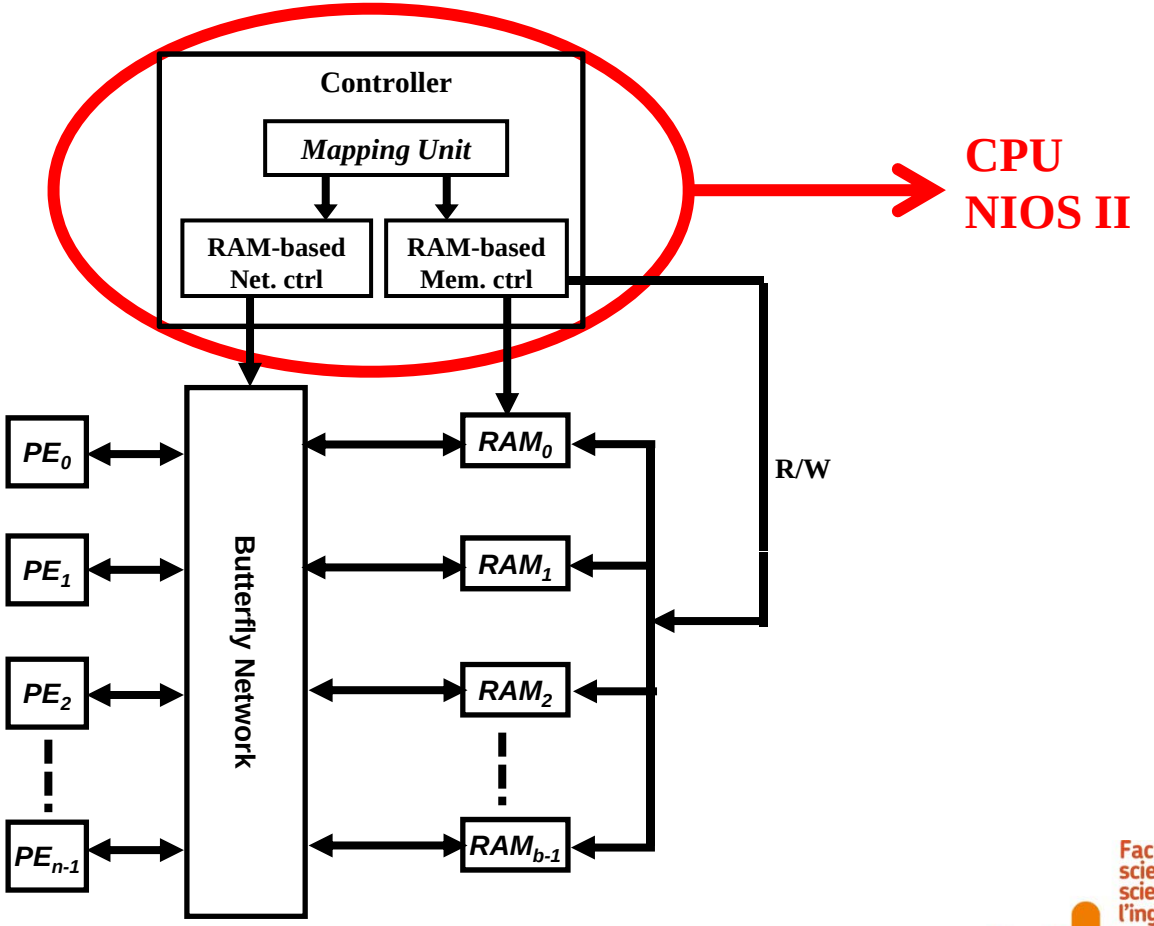
Experiments

GRAAL target system

- **First experiments performed on a CPU**



HSPA interleaver for 3GPP-WCDMA standard

- **FPGA target : ALTERA Cyclone-III with NIOS II embedded processor**
- **Processor clock frequency of 195MHz**
- **Software Mapping Unit** (runs on embedded processor)

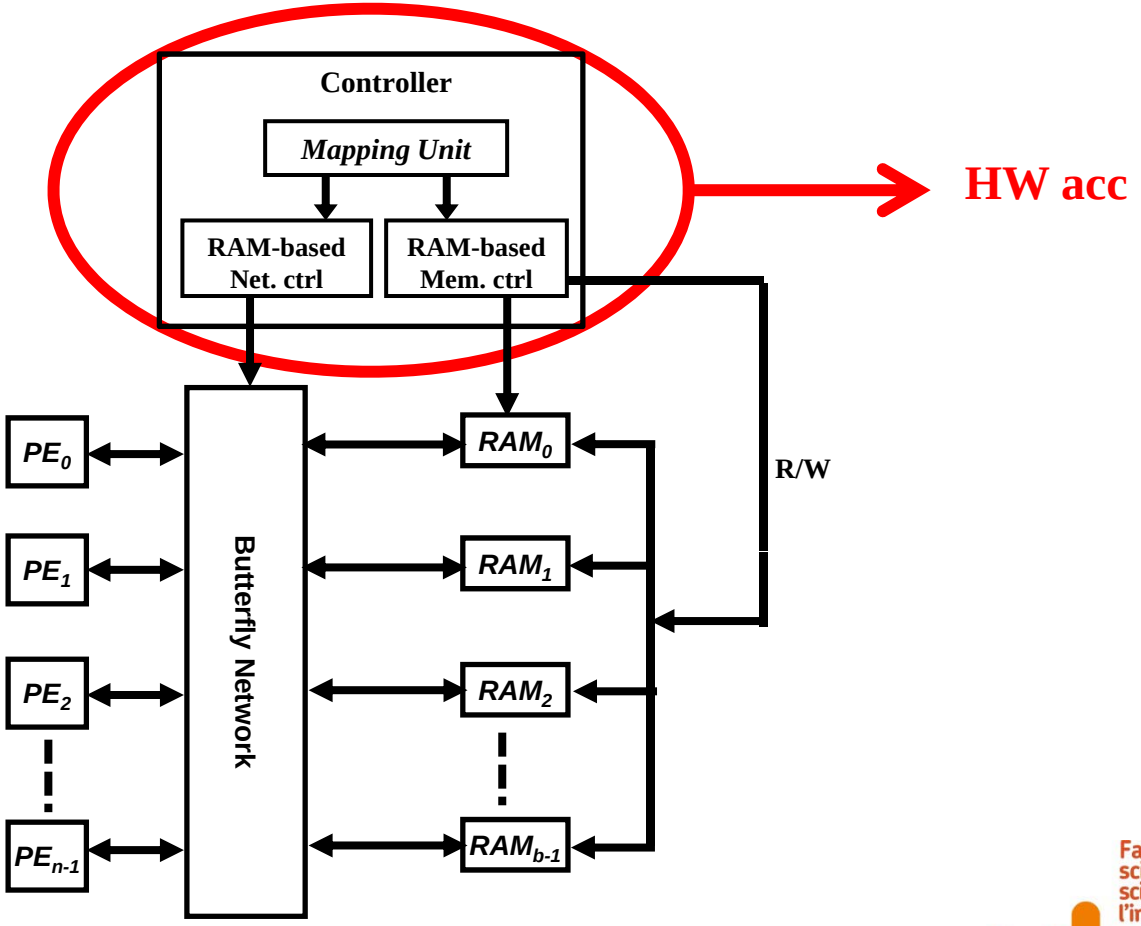
Block Length	256				1024				2048			
Parallelism	4	8	16	32	4	8	16	32	4	8	16	32
Time (in Seconds)	**0,01**	**0,02**	**0,03**	**0,03**	**0,05**	**0,08**	**0,11**	**0,16**	**0,11**	**0,17**	**0,24**	**0,33**
Block Length	3072				4096				5120			
Parallelism	4	8	16	32	4	8	16	32	4	8	16	32
Time (in Seconds)	**0,17**	**0,24**	**0,36**	**0,51**	**0,23**	**0,35**	**0,49**	**0,71**	**0,35**	**0,42**	**0,61**	**0,87**

- **Best mapping latency : 10 ms (block length 256 & parallelism of 4)**
- **VHDL prototyped with parallelism 8**

S. Ur Rehman, A. Sani, P. Coussy and C. Chavet, "Embedding Polynomial Time Memory Mapping and Routing Algorithms on-chip to Design Configurable Decoder Architecture", In Proceedings of **IEEE International Conference on Acoustics, Speech and Signal Processing**, Florence, May, 2014.

GRAAL target system

- **Hardwired implementation**



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HSPA interleaver for 3GPP-WCDMA standard

- **FPGA target : ALTERA Cyclone-III**
- **Clock frequency of 100MHz**
- **Hardware Mapping Unit** (PE parallelism = 8)

Block Length	256	1024	2048	3072	4096	5120
CPU *(clock 195MHz)*	20	80	170	240	350	420
ASIC *(clock 100MHz)*	0,019	0,076	0,153	0,23	0,307	0,384

Time given in *msec* for both

- **SpeedUp ~1000 and reduced frequency**
- **These latencies are in compliance with HSPA standard that requires 50 to 100 ms of latency for call setup and data transfer**

A.H. Sani, C. Chavet and P. Coussy, "A Dynamically Reconfigurable ECC Decoder Architecture", In Proceedings of **IEEE International Conference on Design And Test in Europe**, Dresden, march 2016

Dissemination

- **Patent and Technological maturation funded by *SATT Ouest Valorisation***
- **Book, chapter and papers**
  - C. Chavet and P. Coussy Eds, "Advanced Hardware Design for Error Correcting Codes", Springer-Verlag (2015)
  - IEEE Transaction on Signal Processing (2013)
  - IEEE ICASSP (2014)
  - IEEE DATE (2016)
- **Two PhD thesis, one Post-Doc and one research engineer**

Conclusion

Conclusion

- **GRAAL Patented Architecture specification is based on two main processing steps**
  - Online generation of a virtual conflict free memory mapping
  - Online generation control words from the virtual mapping
- **GRAAL Architecture Vs "Classical" adaptive approaches**
  - Control memories (set of ROMs) for multi-mode systems are replaced by smaller RAMs
  - Simplified implementation of Euler partitioning algorithm with network control word generation (*not presented today*)
- **A VHDL prototype has proven its efficiency on FPGA targets, and we plan to finalize an ASIC prototype**
- **This architecture must be launched into the *Real World…*** *or at least prove its ability and flexibility with industrial applications*

Collaborations are welcome!!

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